

Fig. 1A PRIOR ART

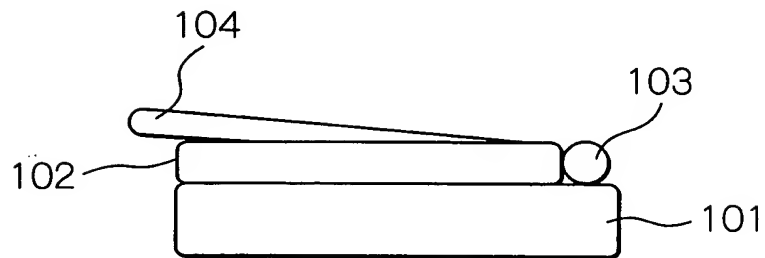
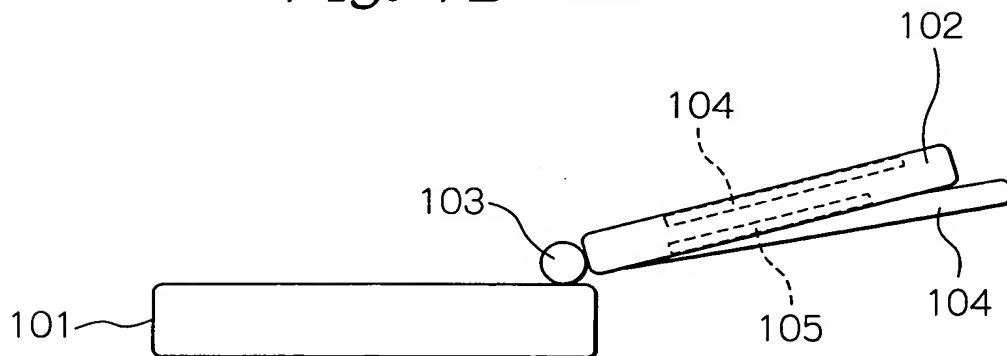


Fig. 1B PRIOR ART



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Fig. 1C
PRIOR ART

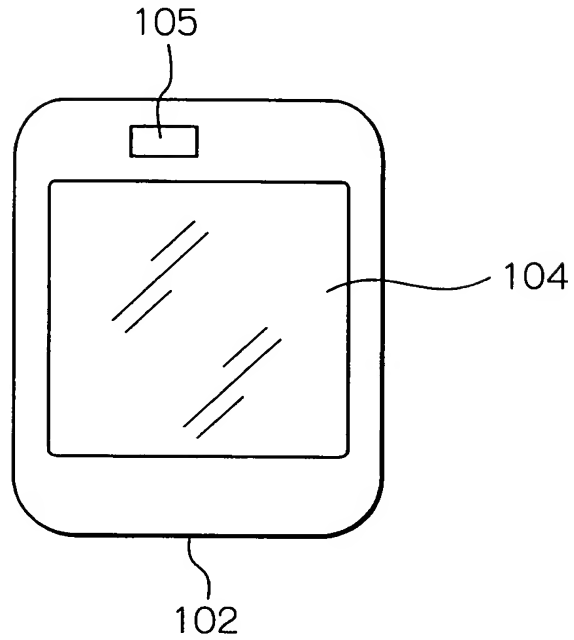
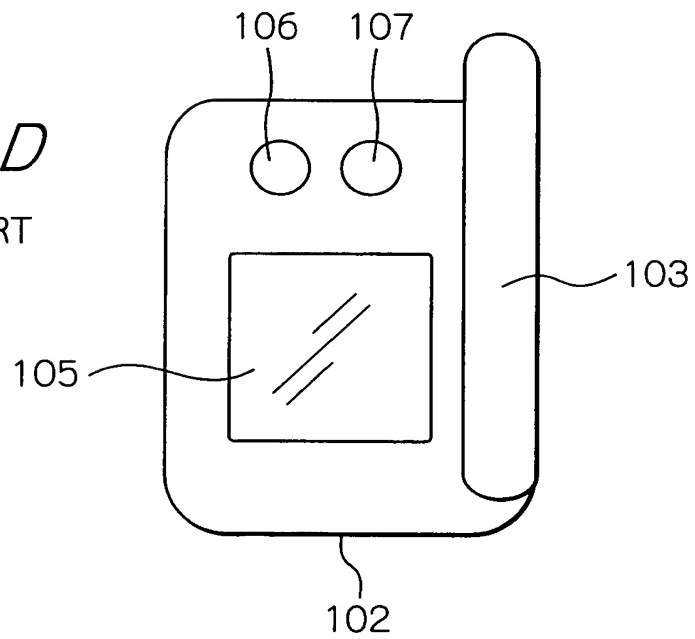
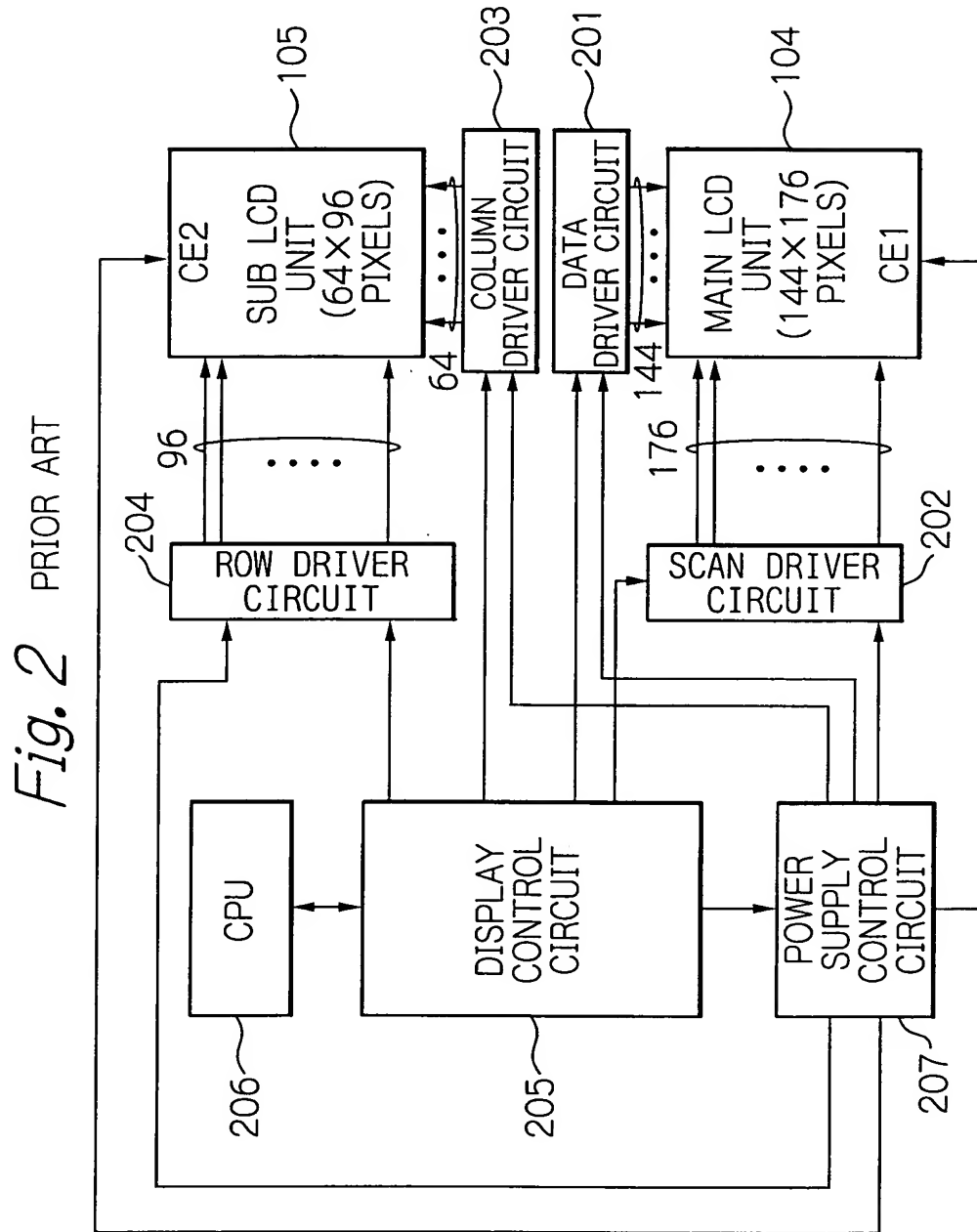


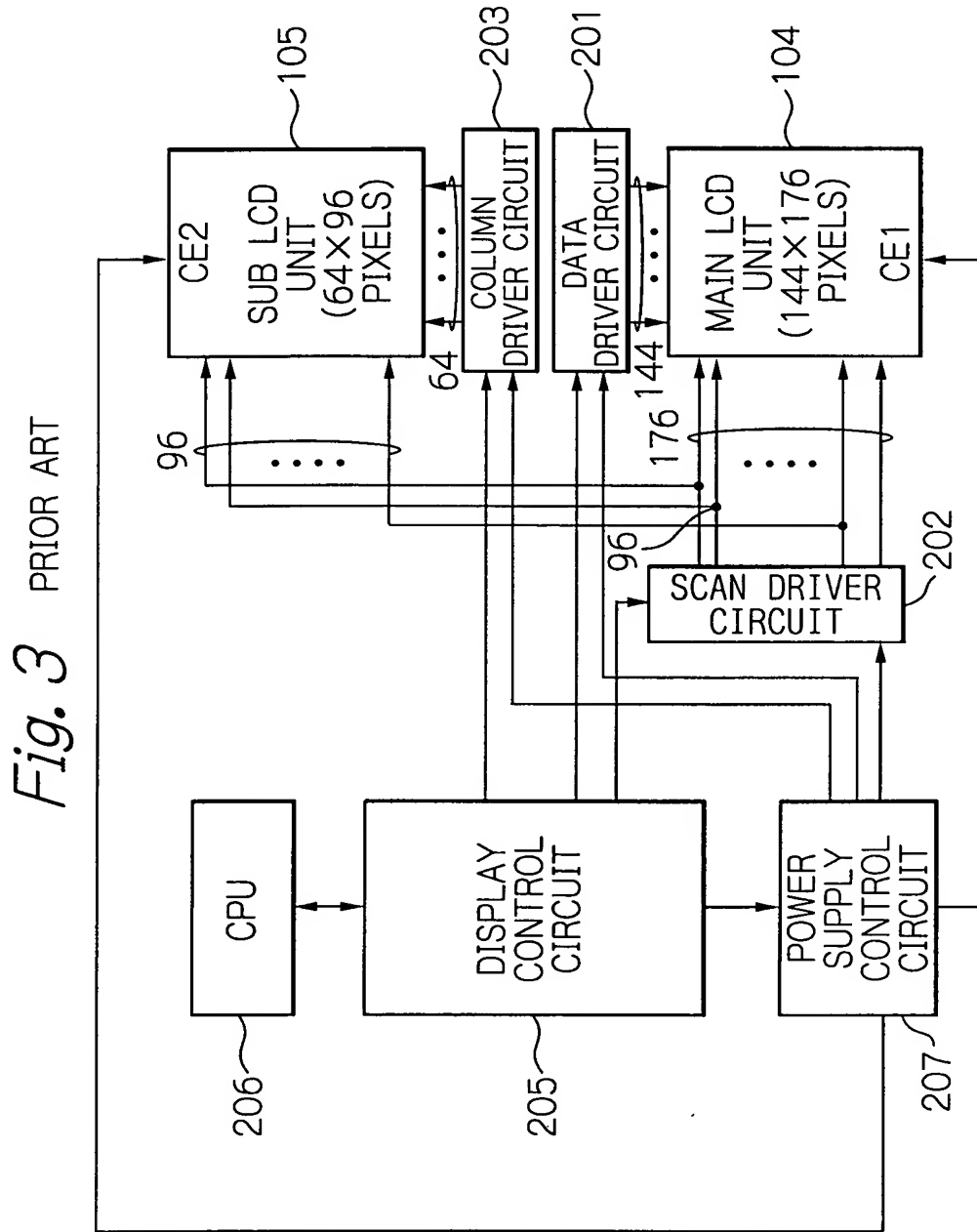
Fig. 1D
PRIOR ART



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Fig. 4

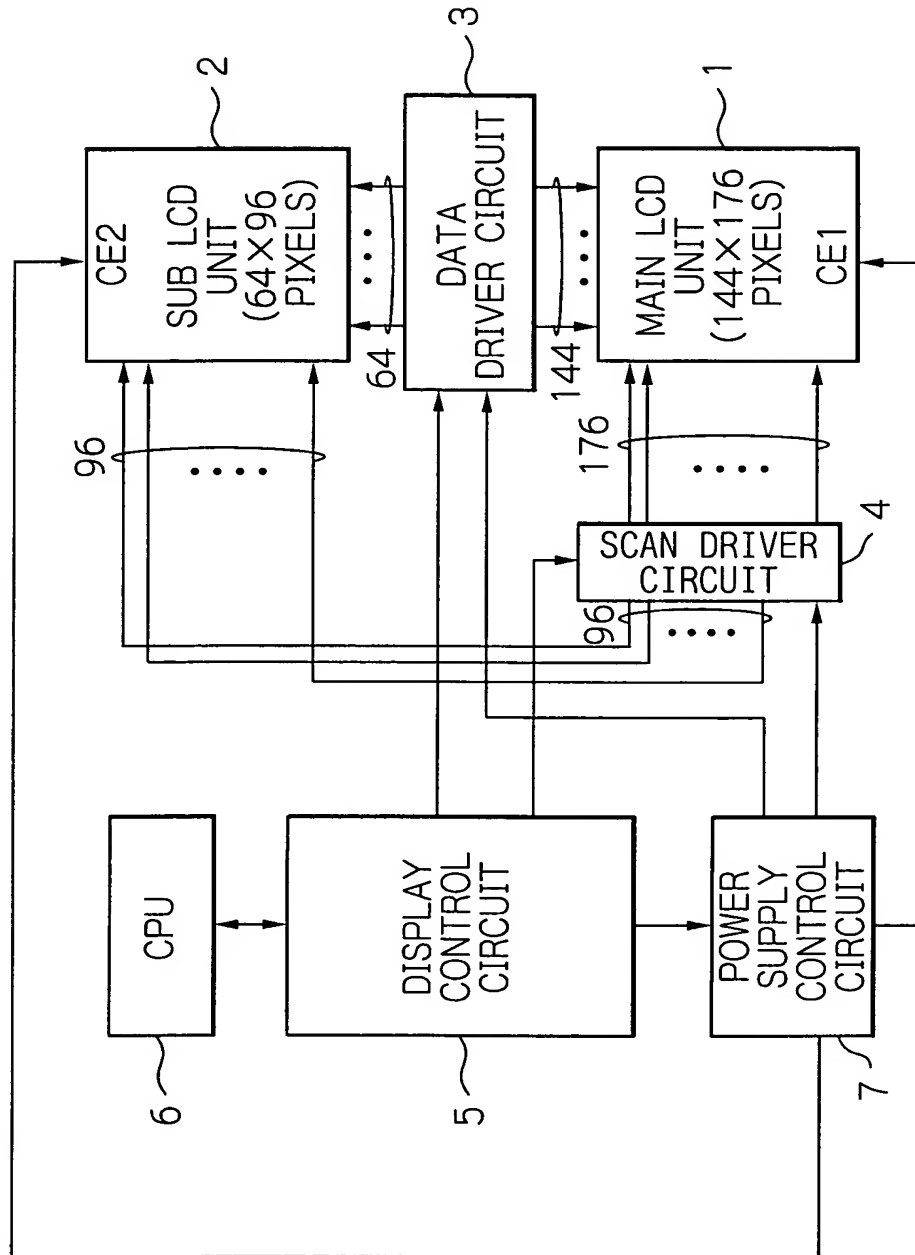


Fig. 5

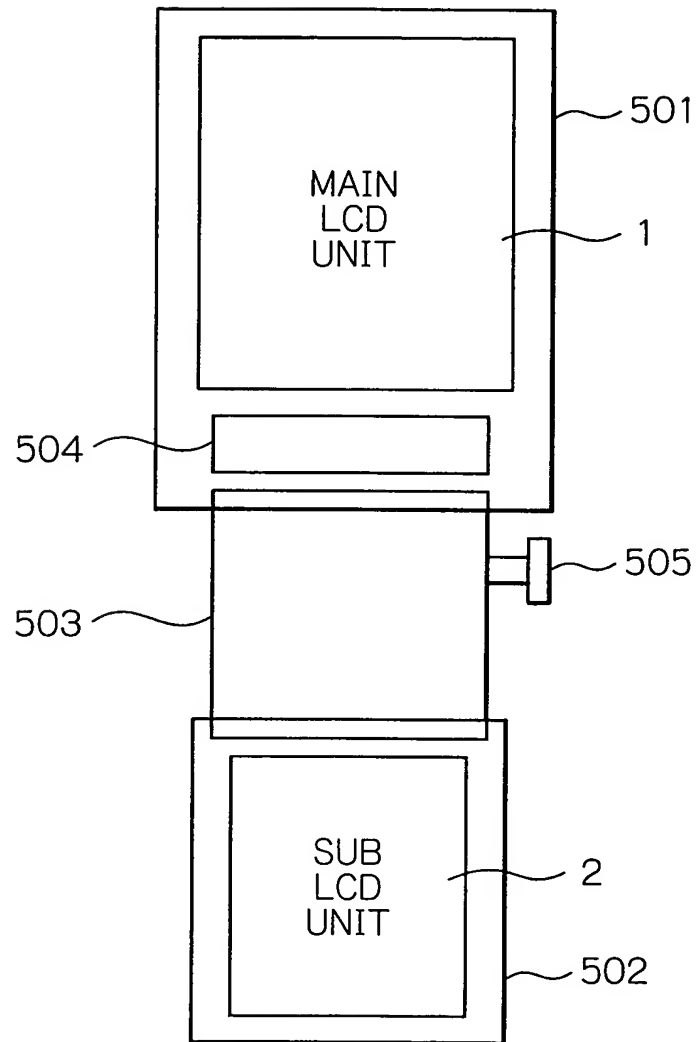
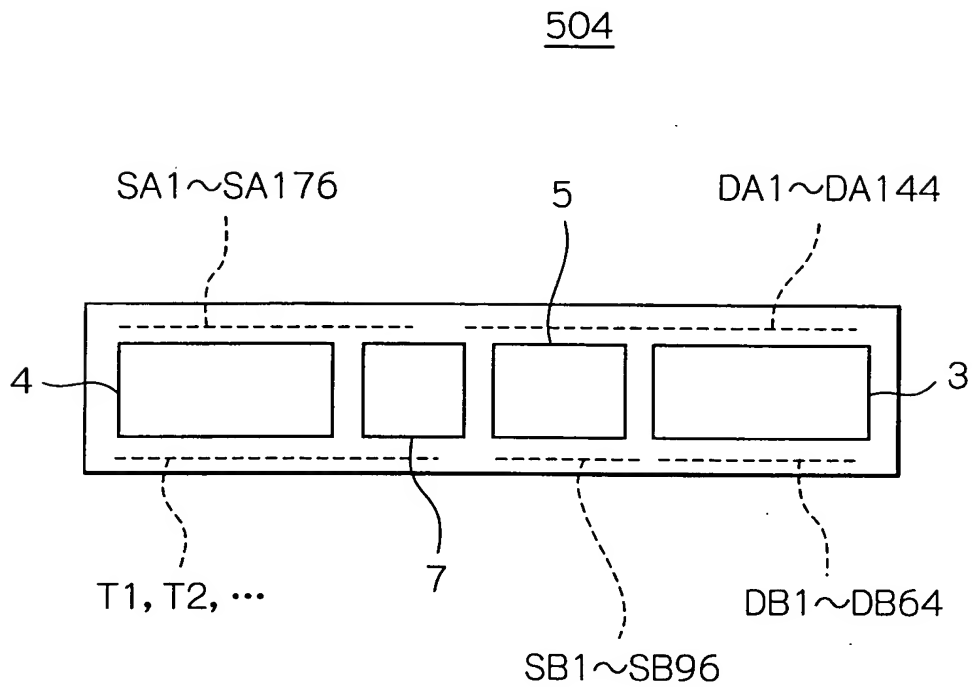
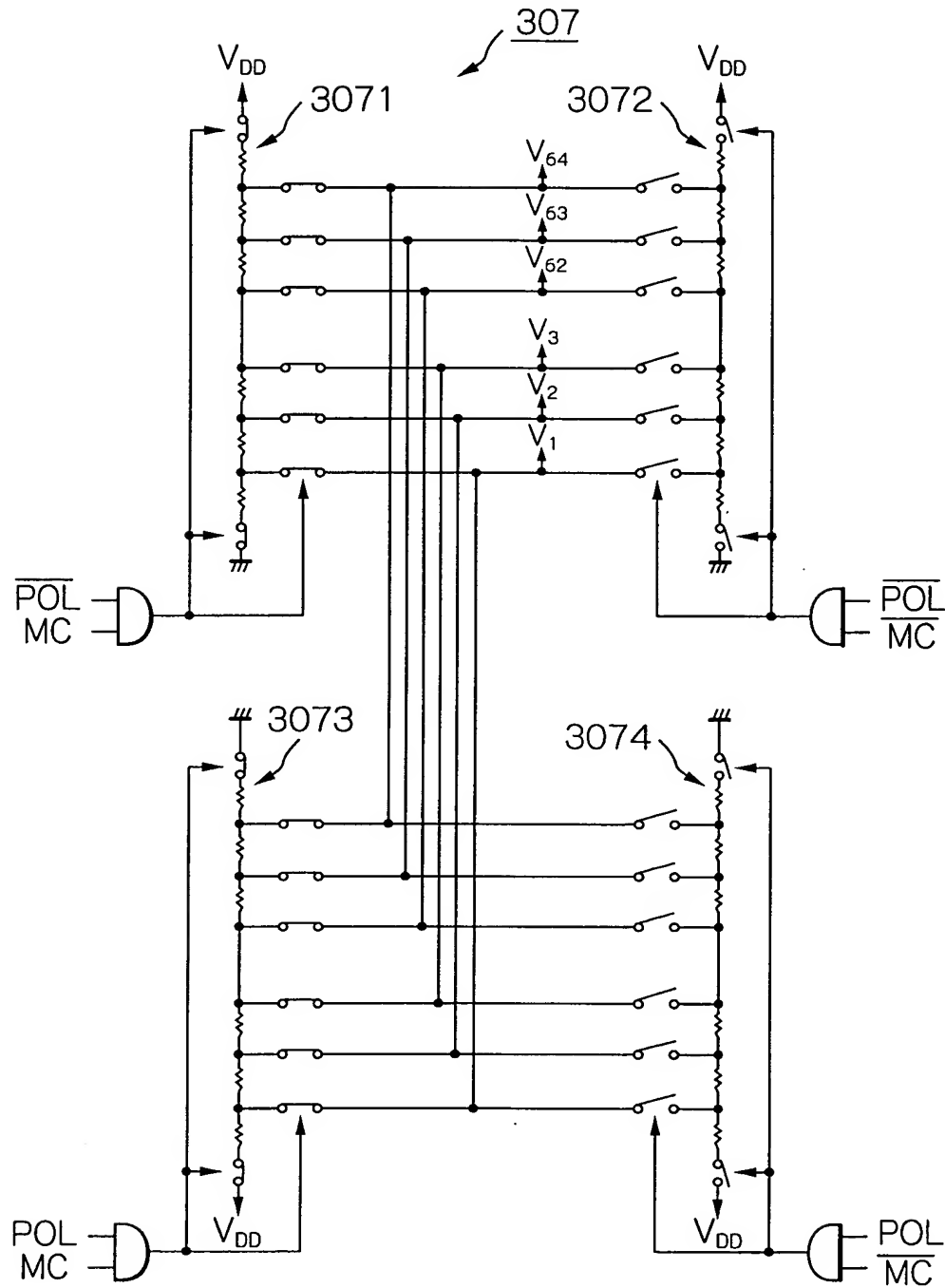


Fig. 6



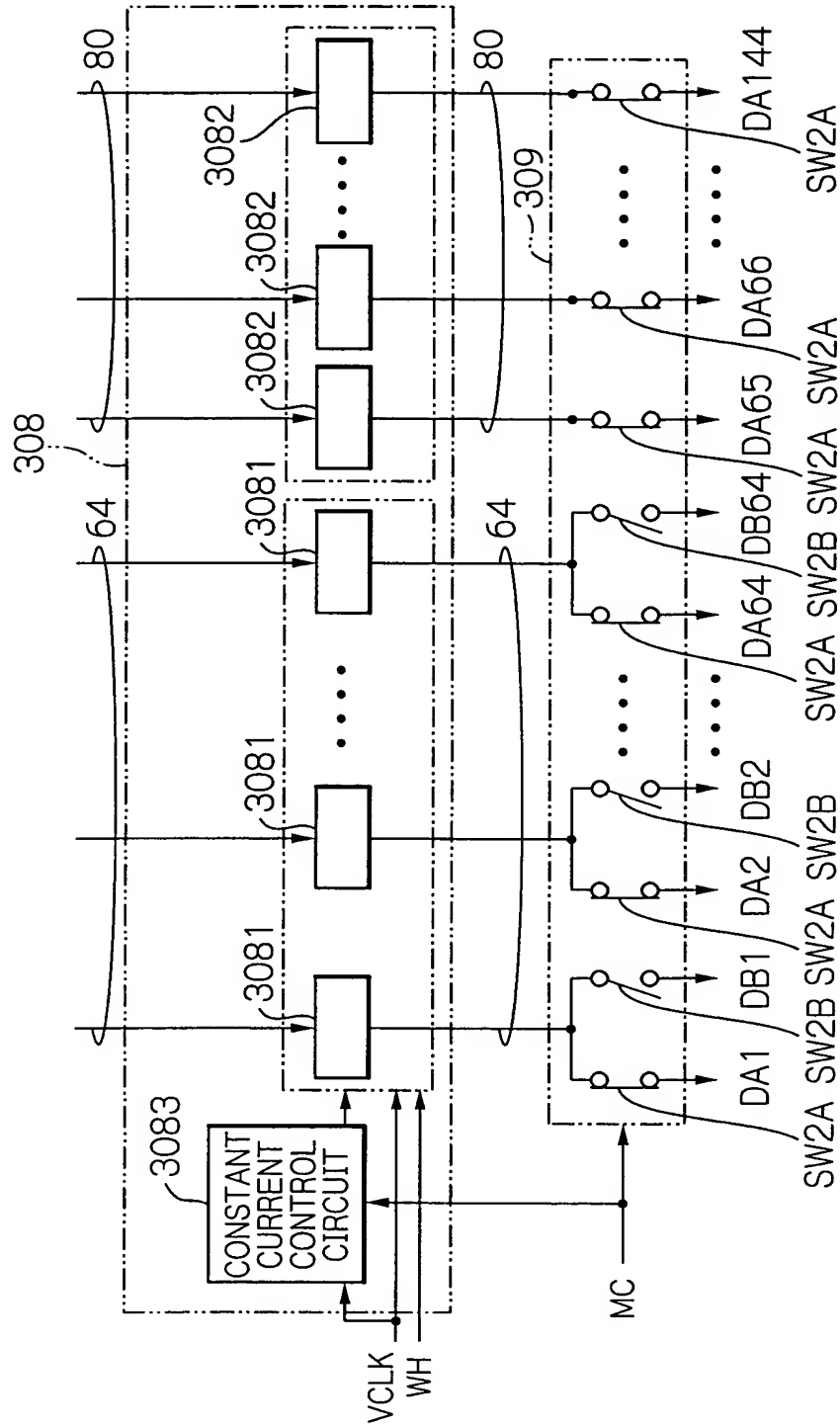
The diagram illustrates a video signal processing circuit 5. It is divided into two main functional blocks: 311A and 301B. Block 311A contains the MAIN FRAME MEMORY, SUB FRAME MEMORY, and a GRADATION VOLTAGE GEN. CIRCUIT. Block 301B contains the LINE MEMORY, LINE MEMORY, LEVEL SHIFT CIRCUIT, DECODER CIRCUIT, and OUTPUT CIRCUIT. The circuit is controlled by signals RW, D0~Dn, ADC, MS, LAT1, LAT2, POL, VCLK, WH, and MC. Data is output as DAI, DBI, and DAJ. The circuit includes various switches (SW1A, SW1B, SW2A, SW2B) and buffers (144, 64, 80).

Fig. 8



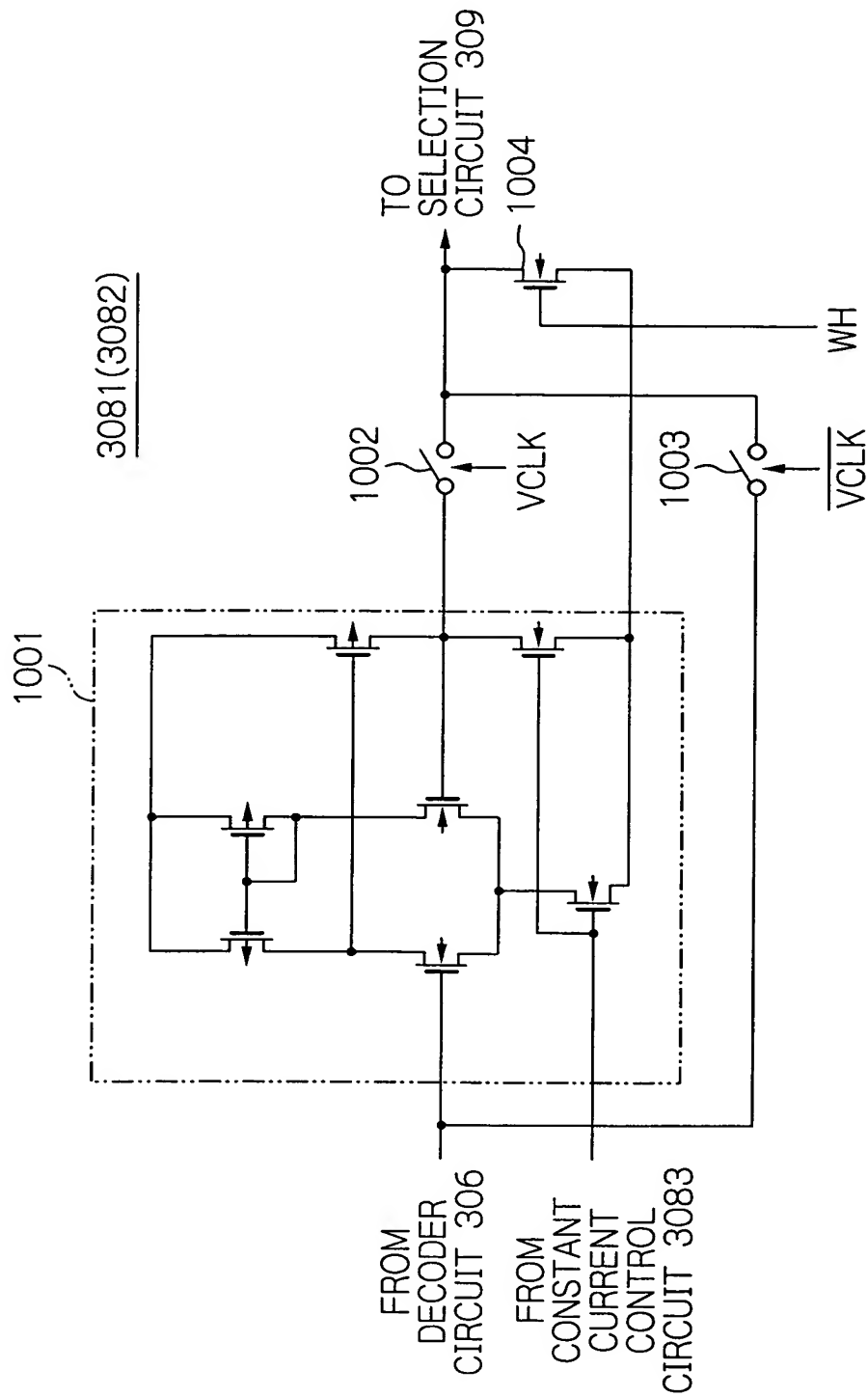
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Fig. 9

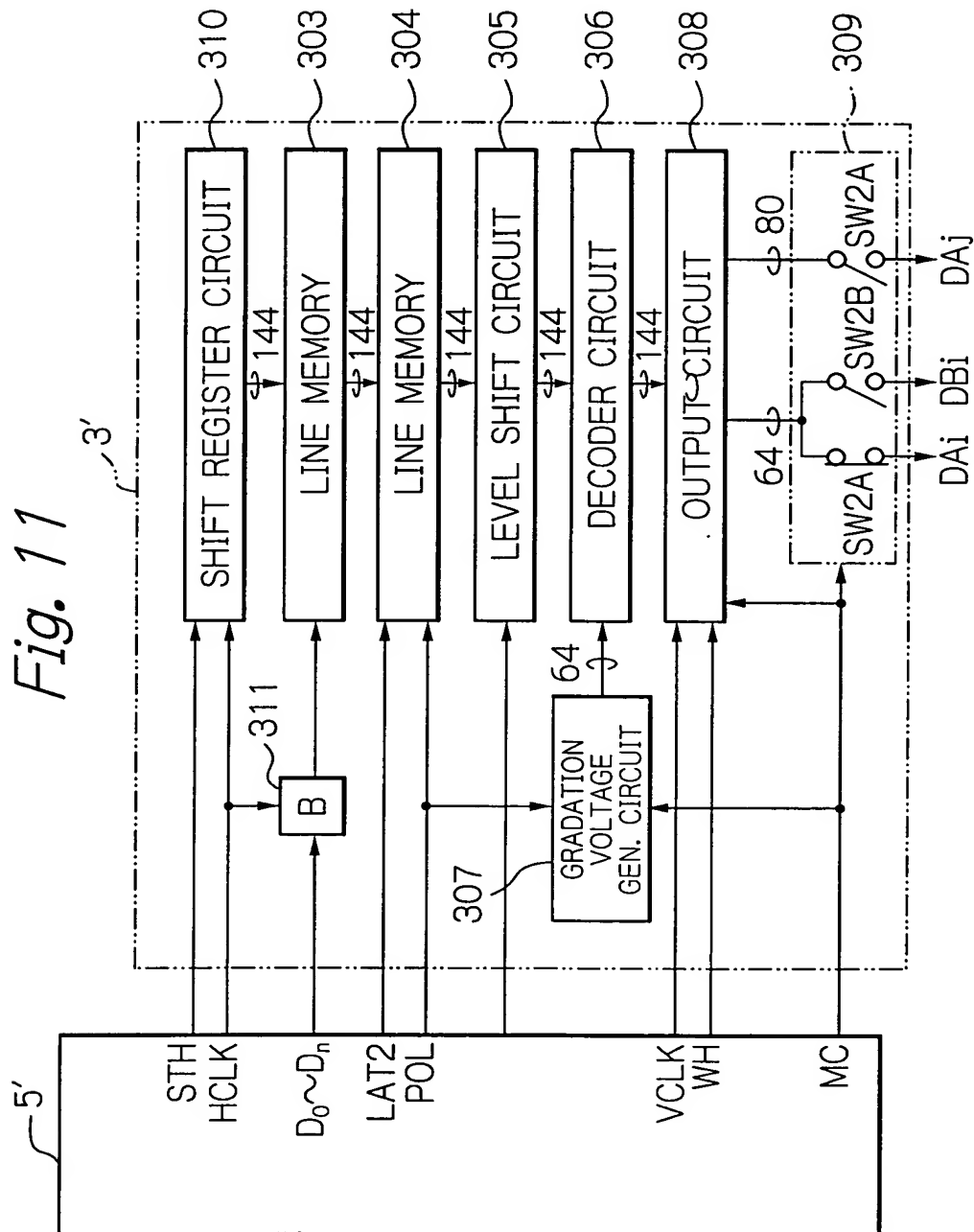


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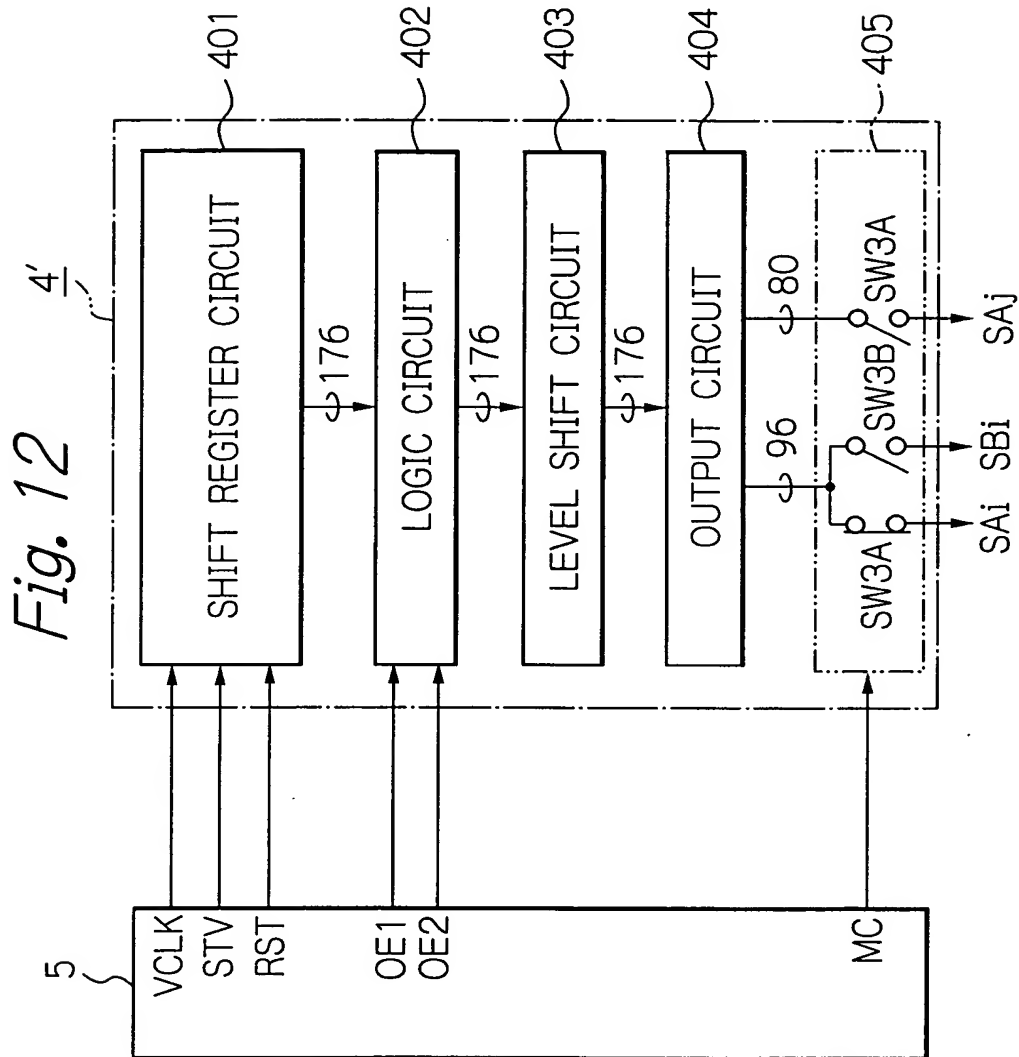
Fig. 10



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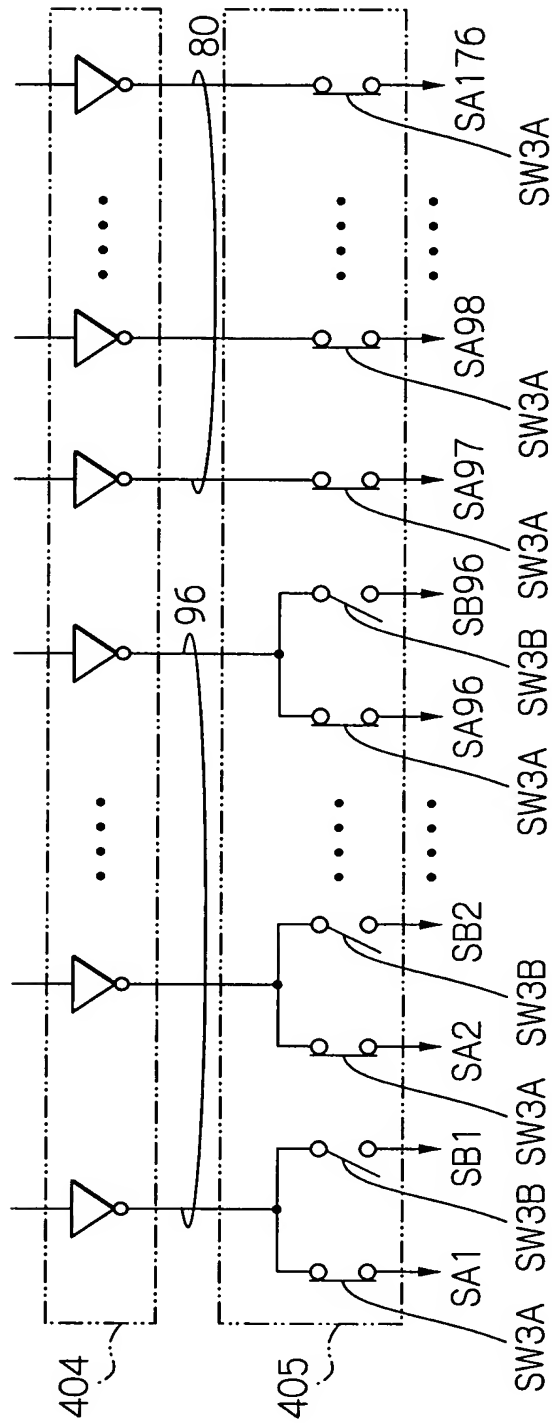


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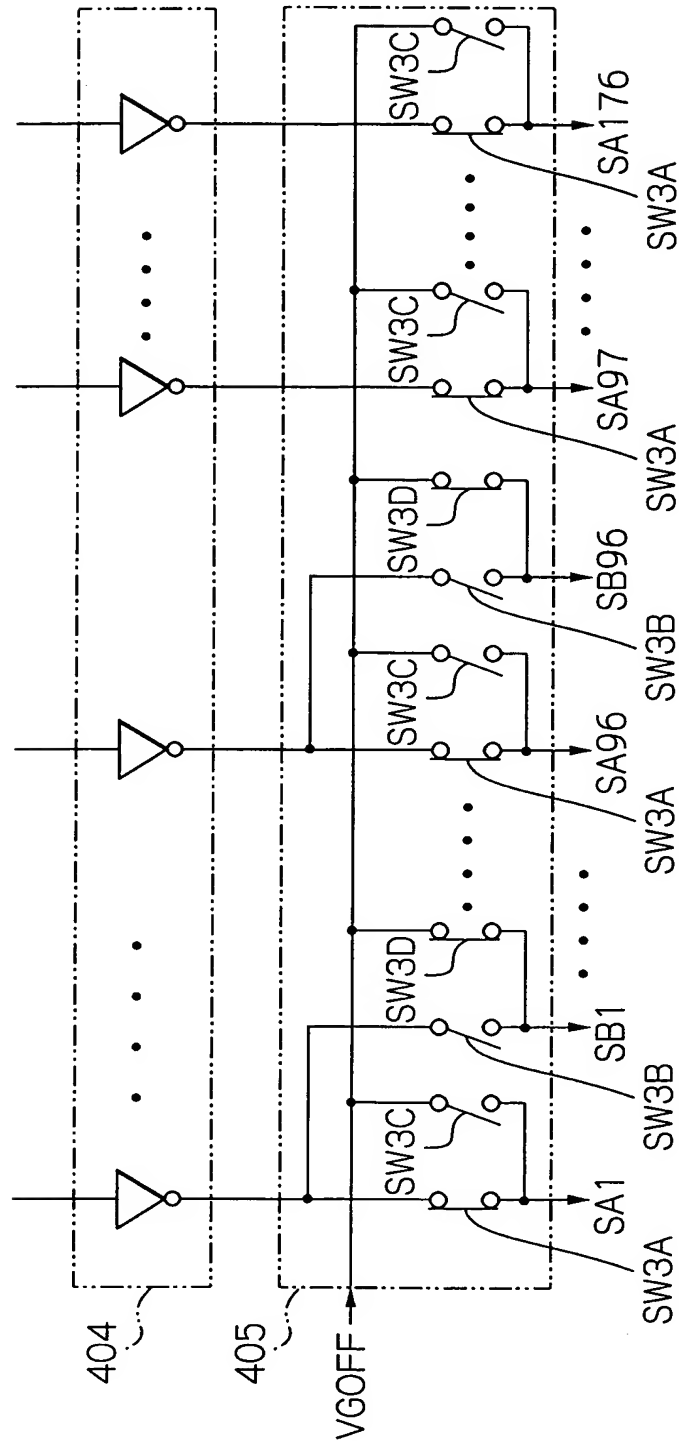
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Fig. 13



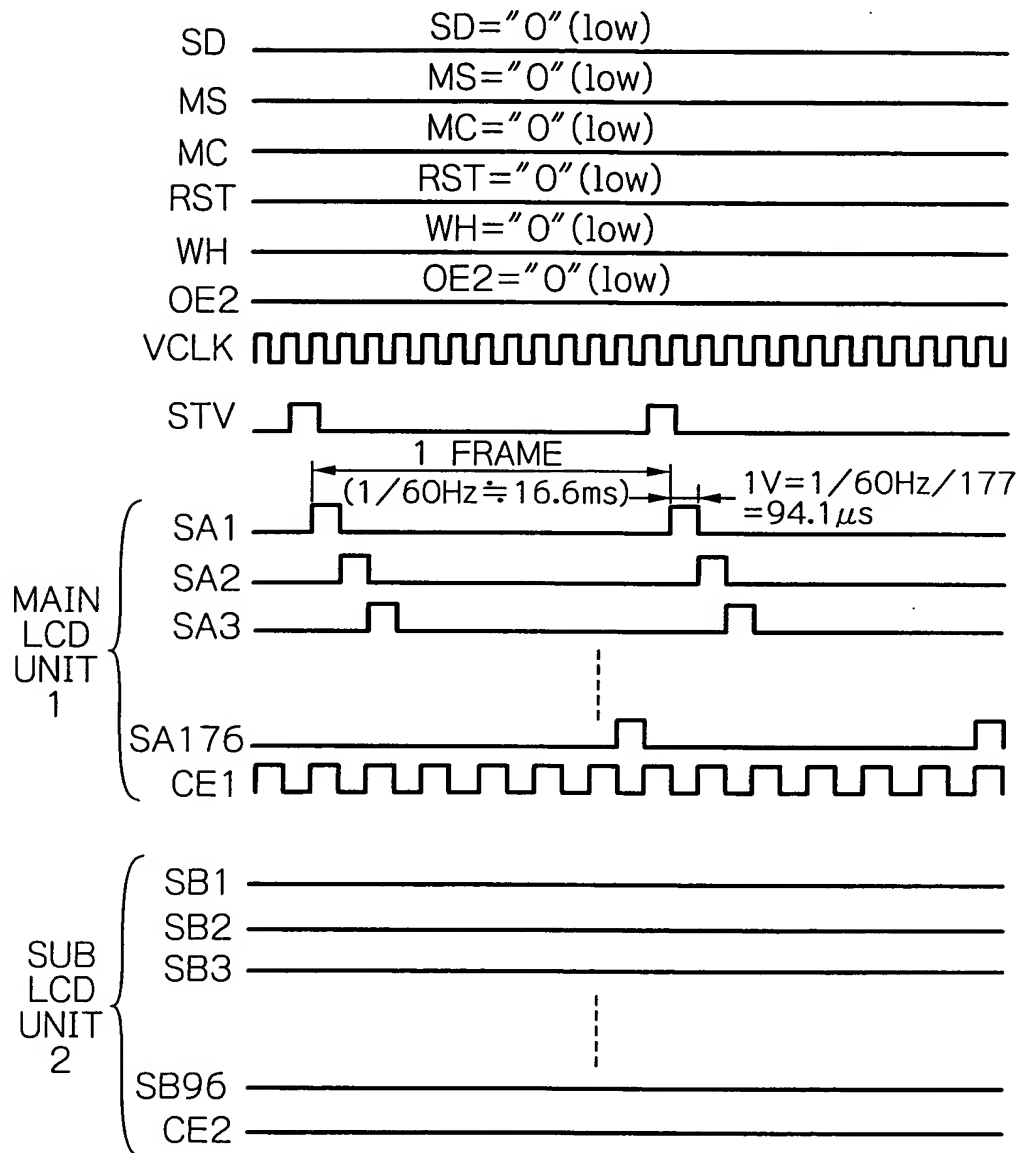
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Fig. 14



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Fig. 15



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Fig. 16

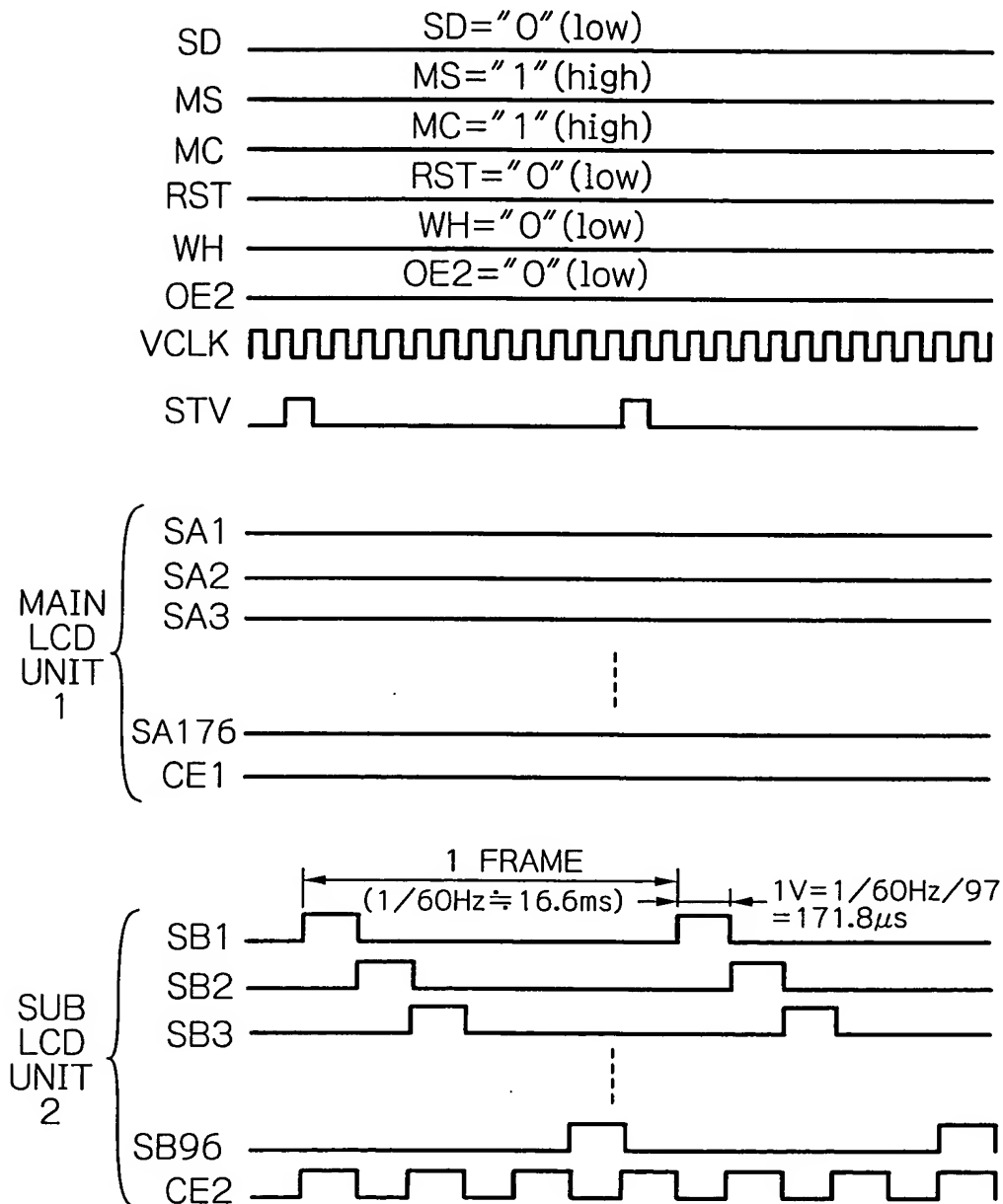


Fig. 17

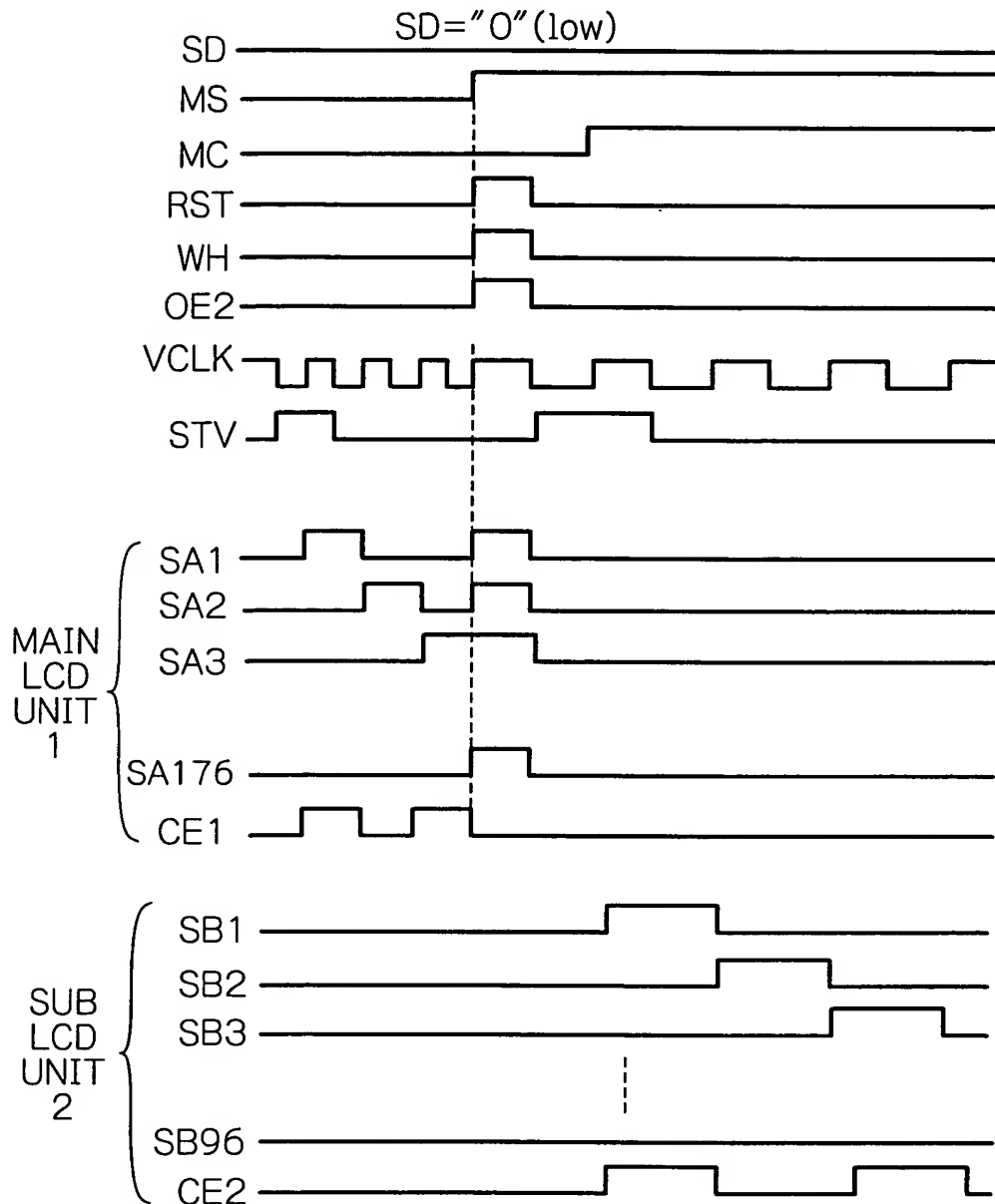
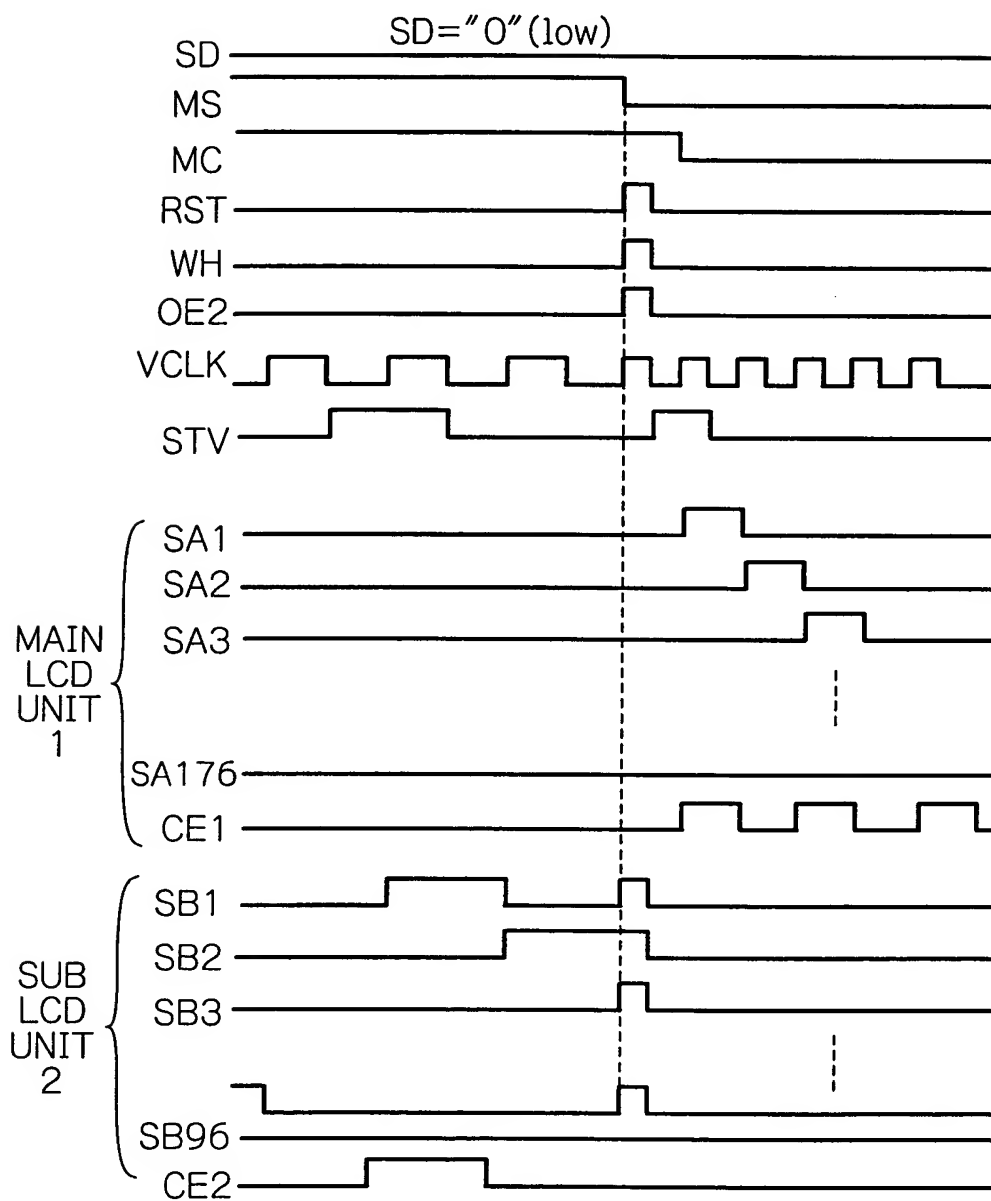
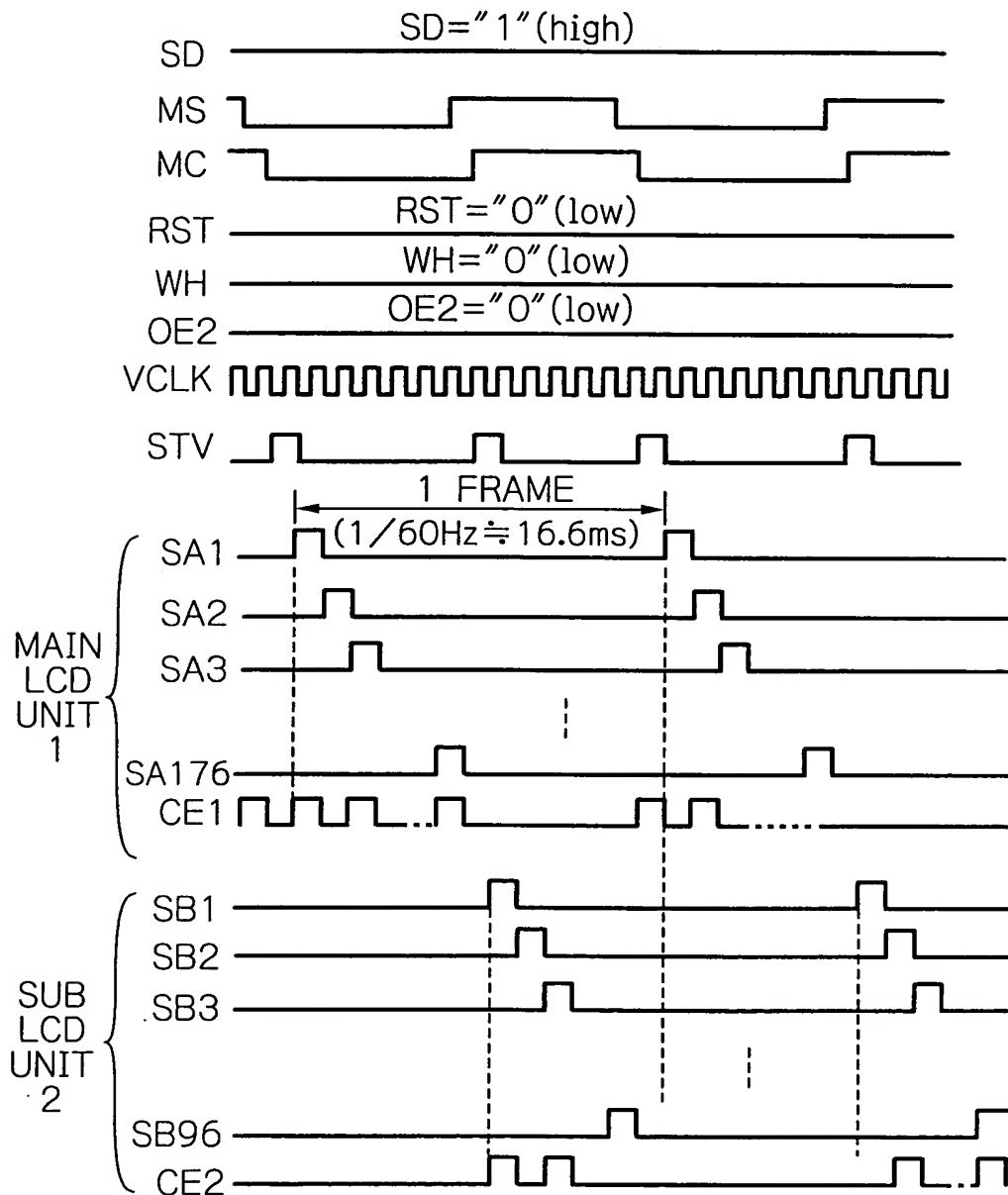


Fig. 18



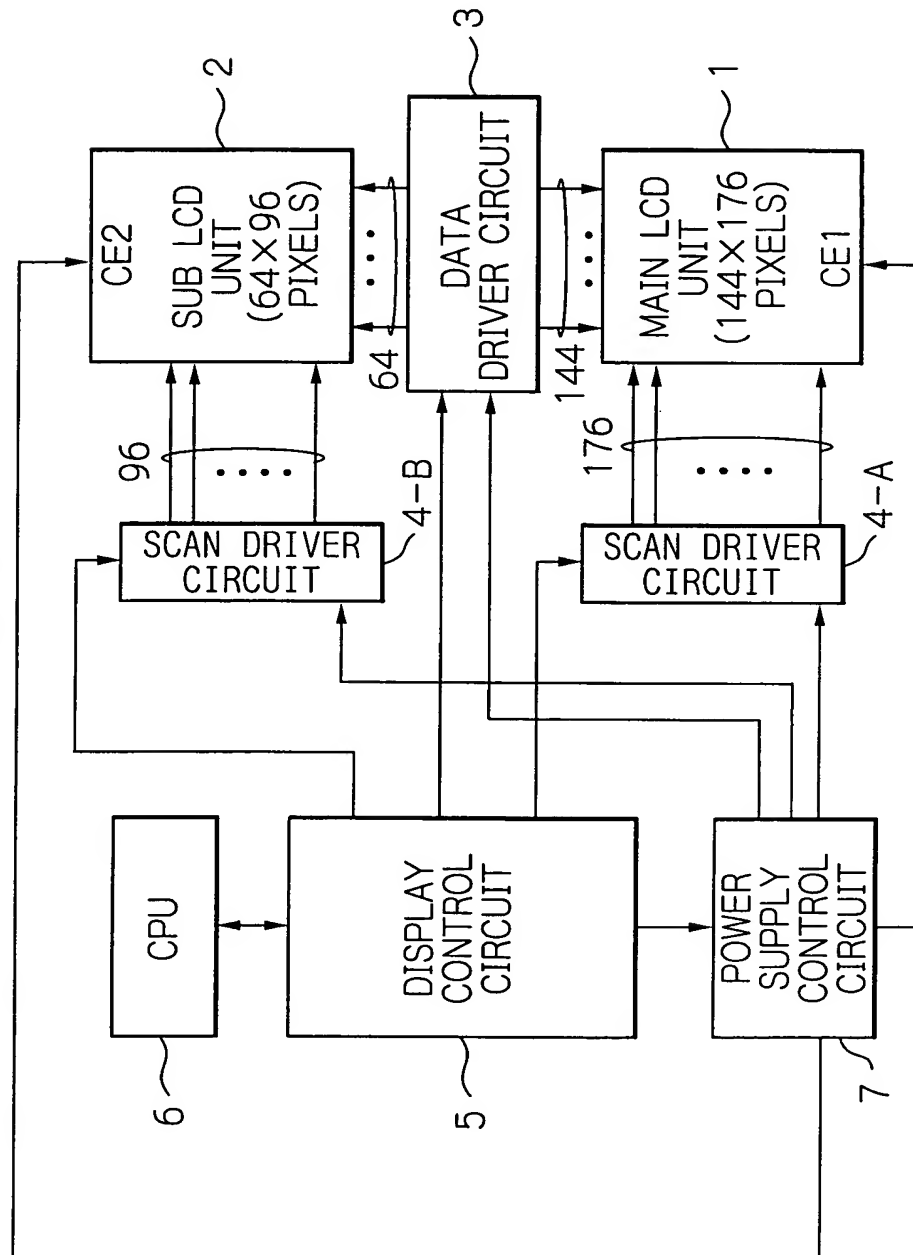
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Fig. 19



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Fig. 21



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Fig. 22A

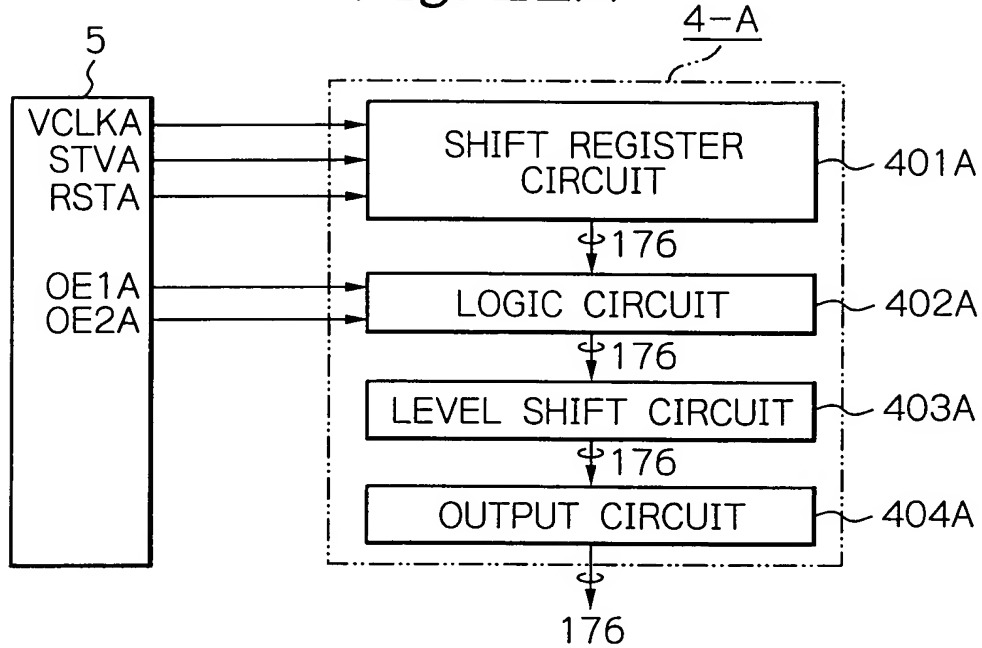
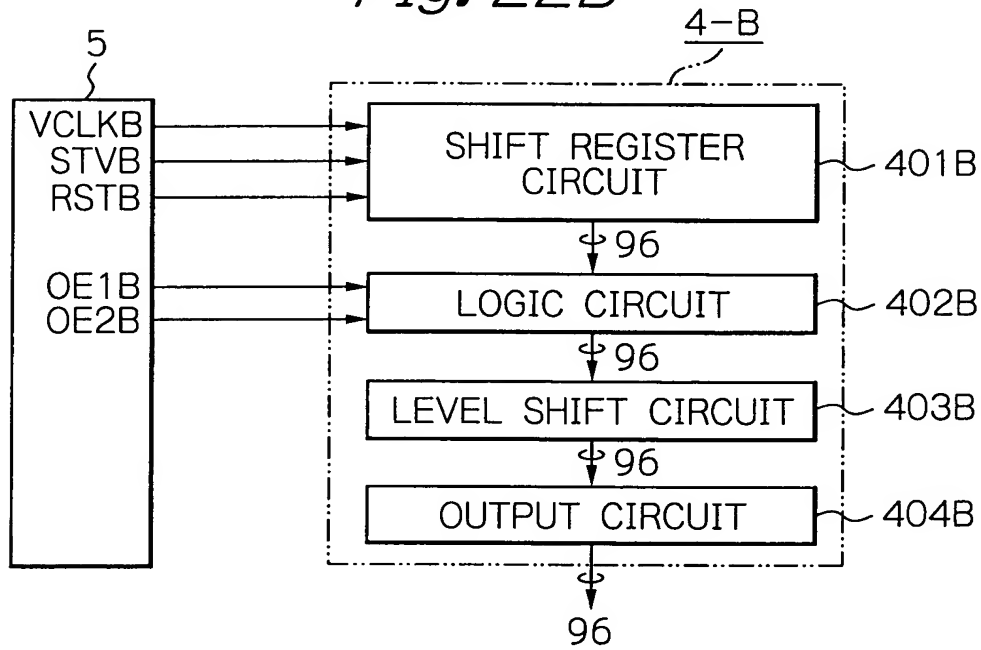
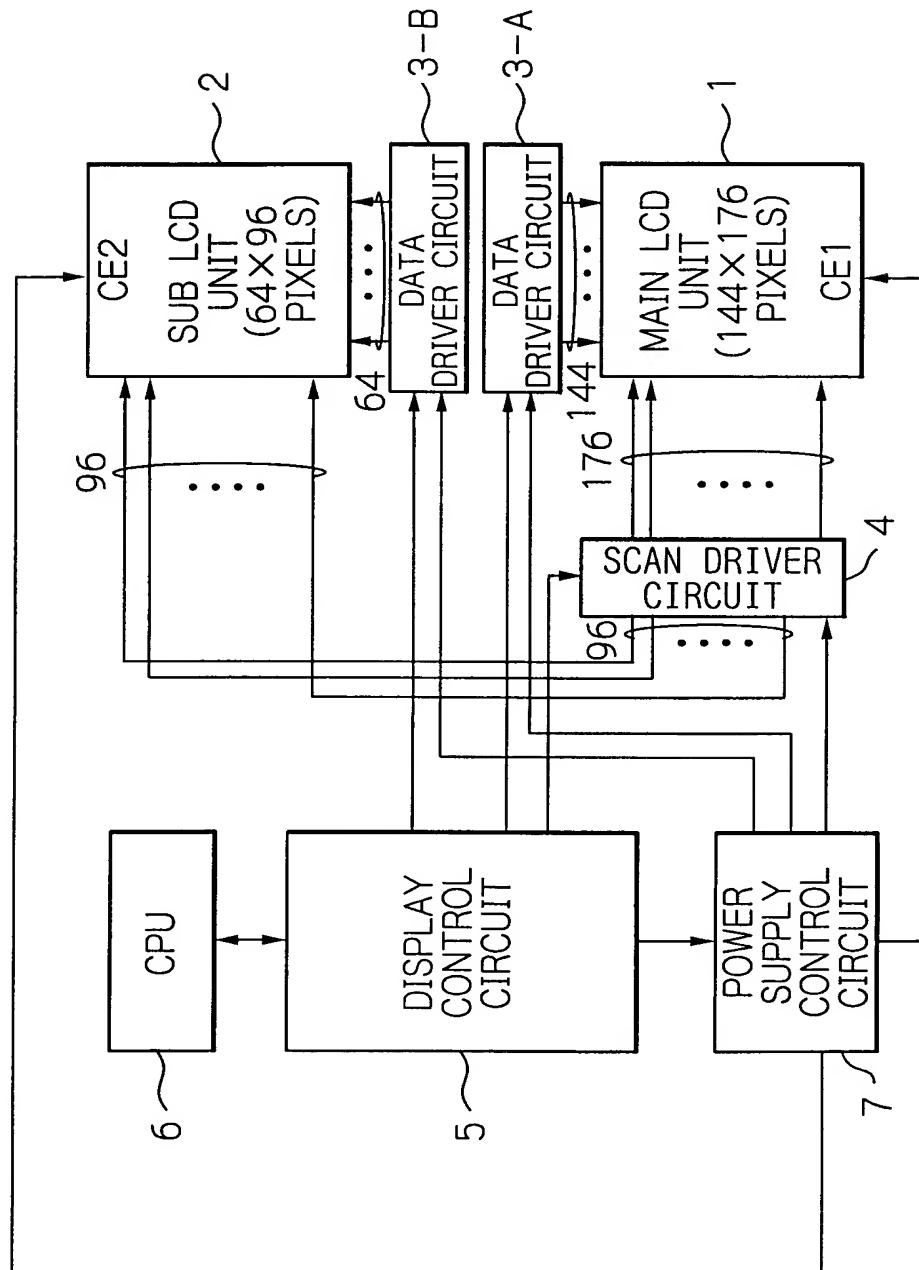


Fig. 22B

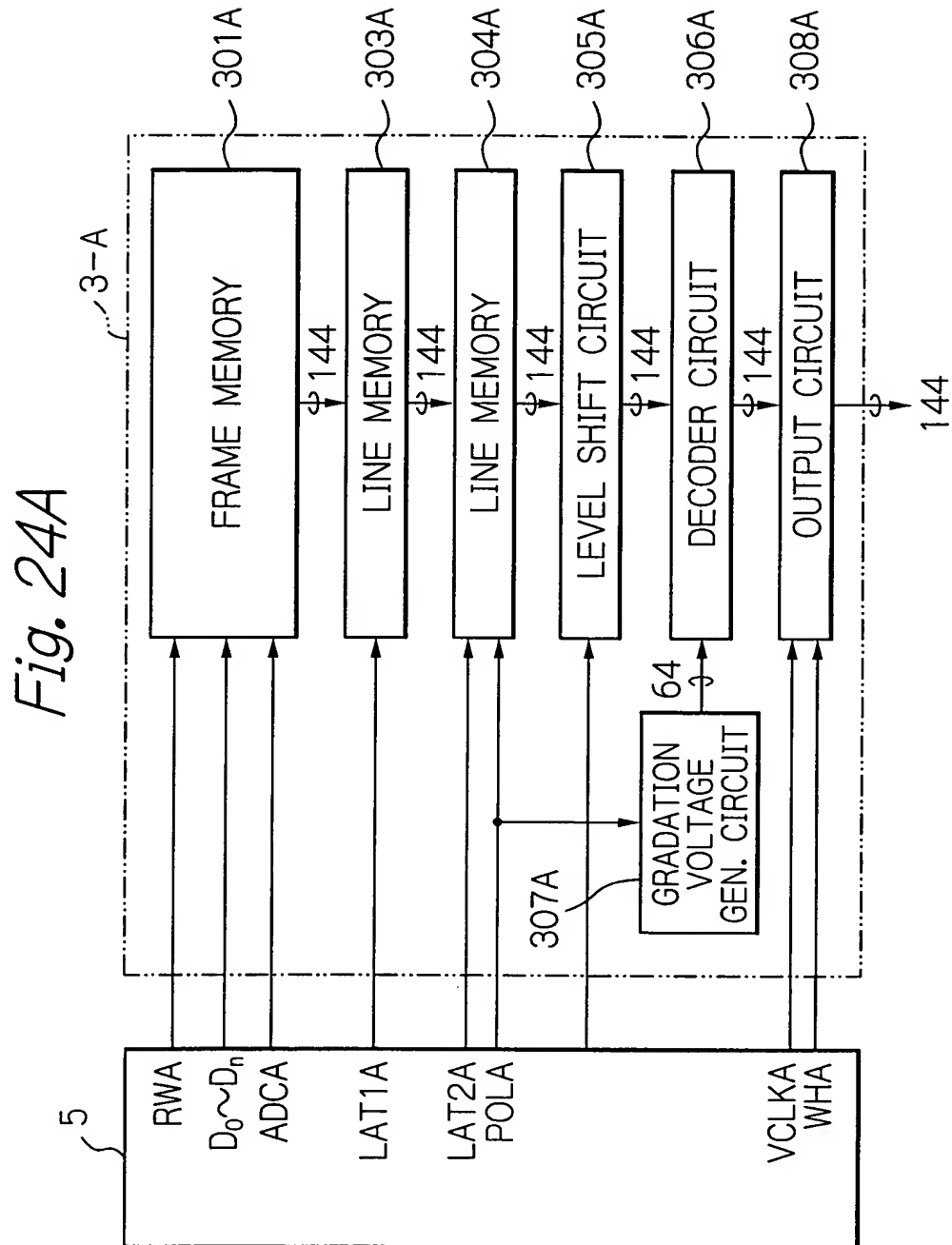


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Fig. 23



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